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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,055	10/14/2003	Kaushik Kumar	2003 P 53141 US	5717

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,055	KUMAR ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *25-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 18-24* is/are rejected.

7)☒ Claim(s) *14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/25/05, 7/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I (claims 1-24) in the reply filed on 7/19/2005 is acknowledged.

Specification

The disclosure is objected to because of the following informalities: In paragraph 1, line 2, "xx/xxx,xxx" must be replaced with a serial number.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 8 recites the limitation "first conductive lines" in line 3. There is insufficient antecedent basis for this limitation in the claim. For the purposes of patentability, the examiner assumes that the "first conductive lines" are the "conductive lines formed in a dielectric layer" recited in line 2 of claim 7, which are the same "conductive lines" recited in line 1 of claim 8.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10, 13, 18, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Bekiaris et al. (U.S. 2003/0119307), using Applied Materials' data sheet for Black Diamond™ to establish inherency for claim 8.

Regarding claim 1, Bekiaris et al. teaches a method of fabricating a semiconductor device, the method comprising providing a workpiece (Fig. 5A, paragraph 0022); disposing a first dielectric material over the workpiece (**114** in Fig. 5B, paragraph 0036); disposing a second dielectric material over the first dielectric material (**116** in Fig. 5B; paragraph 0036), the second dielectric material comprising a different material than the first dielectric material (paragraph 0036), wherein the first dielectric material and the second dielectric material comprise a first insulating layer (**110** in Fig. 5B); and forming a first pattern in the first dielectric material (**150** in Fig. 5K) and a second pattern in the second dielectric material (**152** in Fig. 5K), the second pattern being different from the first pattern (Fig. 5K).

Regarding claim 2, Bekiaris et al. teaches the method according to claim 1, and further teaches that the second dielectric material comprises a top surface, and further teaches depositing a conductive material over the patterned second dielectric material and the patterned first dielectric material; and removing the conductive material from the top surface of the second dielectric material (paragraph 0038; **90** in Fig. 3).

Regarding claim 3, Bekiaris et al. teaches the method according to claim 2, and further teaches that removing the conductive material from the top surface of the second dielectric material comprises forming conductive lines in the second pattern of the second dielectric material (Fig. 3, paragraph 0033).

Regarding claims 4 and 5, Bekiaris et al. teaches the method according to claim 2, and further teaches that the conductive material forms vias in the first pattern of the first dielectric, wherein the vias comprise substantially vertical sidewalls (Fig. 3, paragraph 0033).

Regarding claims 6 and 7, Bekiaris et al. teaches the method according to claim 4, and further teaches that the workpiece comprises component regions, wherein at least one of the vias makes electrical contact with a component region of the workpiece, and wherein the workpiece component regions comprise a plurality of conductive lines formed in a dielectric layer (paragraph 0035; **104** in Fig. 5 shows one of the conductive lines).

Regarding claim 8, Bekiaris et al. teaches the method according to claim 7, and further teaches that the conductive lines comprise copper (paragraph 0035), wherein disposing the first dielectric material comprises disposing a material having a coefficient of thermal expansion close to the coefficient of thermal expansion of the first conductive lines (paragraph 0036 teaches that the first dielectric layer is made of Black Diamond™, which Applied Materials teaches is appropriate for use in copper damascene applications, citing compatible thermal expansion with copper as a criterion, see Applied Materials' data sheet).

Regarding claim 9, Bekiaris et al. teaches the method according to claim 1, and further teaches depositing a hard mask over the second dielectric material (120 in Fig. 5C);

Regarding claim 10, Bekiaris et al. teaches the method according to claim 9, and further teaches that depositing the hard mask comprises depositing a first mask layer (**122** in Fig. 5C); depositing a second mask layer over the first mask layer (**124** in Fig. 5C); and depositing a third hard mask layer over the second mask layer (**126** in Fig. 5C).

Regarding claim 13, Bekiaris et al. teaches the method according to claim 10, and further teaches that forming the first pattern and the second pattern comprises:

patterning at least the third mask layer with the second pattern (Fig. 5F);

patterning the third mask layer, the second mask layer, and the first mask layer with the first pattern (Fig. 5I);

transferring the first pattern to the second dielectric material (**116** in Fig. 5I);

removing the third mask layer, the second mask layer, and the first mask layer in the second pattern regions (Fig. 5K);

transferring the first pattern to the first dielectric material (**114** in Fig. 5K);

and removing the second dielectric material in the second pattern regions (Fig. 5K).

Regarding claim 18, Bekiaris et al. teaches the method according to claim 13, and further teaches depositing a cap layer (**112** in Fig. 5L) over the workpiece, before disposing the first dielectric material; and transferring the first pattern to the cap layer (Fig. 5L).

Regarding claim 21, Bekiaris et al. teaches the method according to claim 13, and further teaches that forming the first pattern and the second pattern further comprises:

after patterning at least the third mask layer with the second pattern, depositing an anti-reflective coating over the first mask layer (**140** in Fig. 5H; paragraph 0044);

depositing a photoresist layer over the anti-reflective coating (**142** in Fig. 5H; paragraph 0044);

patterning the photoresist with the first pattern (**134** in Fig. 5H; paragraph 0045);

and transferring the first pattern in the photoresist layer to the third mask layer, the second mask layer, the first mask layer, and the second dielectric layer (Fig. 5I; paragraph 0046).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation.

Regarding claim 1, Kihara et al. teaches a method of fabricating a semiconductor device, the method comprising providing a workpiece; disposing a first dielectric material over the workpiece (**204** in Figs. 2 and 3); disposing a second dielectric material over the first dielectric material (**206** in Figs. 2 and 3), the second dielectric material comprising a different material than the first dielectric material (paragraph

0037), wherein the first dielectric material and the second dielectric material comprise a first insulating layer; and forming a first pattern in the first dielectric material (via in layer **204** in Fig. 3C) and a second pattern in the second dielectric material (trench in layer **206** in Fig. 3C), the second pattern being different from the first pattern (Fig. 3C).

Regarding claims 22 and 24, Kihara et al. teaches the method of claim 1, and further teaches that disposing the first dielectric material comprises disposing an inorganic material (paragraph 0037, FSG—further limited by claim 24), and wherein disposing the second dielectric material comprises disposing an organic material (paragraph 0037, SilK—further limited by claim 24).

Regarding claim 23, Kihara et al. teaches the method according to claim 1, and further teaches that disposing the first dielectric material comprises disposing a material that is etchable selective to the second dielectric material (Fig. 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bekiaris et al. (U.S. 2003/0119307) in view of Hsue et al. (U.S. 2003/0044725).

Regarding claim 11, Bekiaris et al. teaches the method according to claim 10 (note 35 U.S.C.102(e) rejection above), but does not teach that depositing the first mask layer comprises depositing SiC_x, SiC_xN_x, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH, wherein

depositing the second mask layer comprises depositing Si_xN_y or SiO_2, and wherein depositing the third mask layer comprises depositing a refractory metal nitride.

Hsue et al. teaches a dual-damascene method with a low-k dielectric layer and multilayer hard mask, the hard mask layers comprising SiC, SiN, SiO_2, or a refractory metal nitride, TaN (paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Bekiaris et al. and also taught by claim 10, and further form the first hard mask layer of SiC, the second hard mask layer of SiN or SiO_2, and the third hard mask layer of TaN, since Hsue et al. teaches that these materials are appropriate to use as hard mask layers in dual-damascene applications involving low-k dielectrics (paragraph 0026).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bekiaris et al. (U.S. 2003/0119307) in view of Hsue et al. (U.S. 2003/0044725) as applied to claim 11 above, and further in view of Soda (U.S. 2003/0054656).

Regarding claim 12, Bekiaris et al. and Hsue et al. together teach the method according to claim 11 (note 35 U.S.C. 103(a) rejection above), but they do not teach a hard mask layer comprising the combination of a layer of SiC_x and a layer of N-SiC_x over the layer of SiC_x.

Soda et al. teaches a dual-damascene method employing a hard mask layer comprised of a layer of SiC_x and a layer of SiCN (paragraph 0121).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Bekiaris et al. and Hsue et al.

together, and further fabricate the first mask layer of a layer of SiC_x and a layer of SiCN, as taught by Soda to be known in the art as appropriate for dual-damascene applications.

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bekiaris et al. (U.S. 2003/0119307) in view of Tsai et al. (U.S. 2002/0164889).

Regarding claims 19 and 20, Bekiaris et al. teaches the method according to claims 18 and 1 (note 35 U.S.C. 102(e) rejection above), but does not teach forming an adhesion film over a top surface of the cap layer, or forming an adhesion film disposed over a top surface of the first dielectric layer.

Tsai et al. teaches forming a cap layer over a semiconductor structure, depositing an adhesion layer over the cap layer, and forming a low-k dielectric over the adhesion layer, and additionally over the first dielectric layer, to improve the adhesion of the low-k layer to the adjacent layer (paragraph 0012).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Bekiaris et al. and Tsai et al. by using the method taught by Bekiaris et al., and also taught by claims 1 and 18, and further form an adhesion film over a top surface of the cap layer and over the top surface of the first dielectric layer in order to improve the adhesion of the dielectric layer to the adjacent layers, as taught by Tsai et al.

Allowable Subject Matter

Claims 14-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art does not teach or suggest, in combination with the other claimed limitations, before removing the second dielectric in the second pattern regions, cleaning the processing chamber while the wafer remains in the processing chamber or moving the workpiece to a clean processing chamber.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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